Parametric Test for Next Generation Semiconductor Technologies

- Overview of imec
- Overview of a semiconductor process flow
  - The need for in-fab parametric wafer test, process defects, action plans
- Overview of the in-fab parametric wafer test setup
  - Dual prober driven by NI tools, PXIe-4135, block diagram, signal routing
- Process experiment / test scenario with NI hardware and software
- Other test scenario’s
- Benchmarked test results PXIe-4135 SMUs
- Data logging / query / analysis
- Future work
Overview of imec

- independent research center for nanotechnology
- key players from semiconductor industry
- partnerships with tools- and material suppliers
- Advanced semiconductor process development
- State of the art 300mm wafer FAB
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Overview of imec: core IA semiconductor programs

- LOGIC program
- Pushing Moore’s law
- new materials/architectures
- From Bulk CMOS to nanowire

Image courtesy: ASML
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Overview of imec: core IA semiconductor programs

- 3D program
  - Stacking ICs / wafers with TSVs
  - 1 single device: performance, power, footprint
  - Multiple 3D integration schemes

Image courtesy: www.i-micronews.com

Heterogeneous integration: extend the number of functions
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Overview of a semiconductor process flow / need for inline electrical test

- Hundreds of dedicated process steps
- R&D environment, complexity $\Rightarrow$ process defects $\Rightarrow$ yield drop (3D)

- Electrical test at early process stage:
  - Very early feedback of device performance
  - Monitoring of processes/tools
  - Rework wafers

$\Rightarrow$ Speed up learning cycle
$\Rightarrow$ Reduced wafer/processing cost
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Overview of a semiconductor process flow / process defects examples

W “dishing” in probe pad areas

W

Si
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Overview of a semiconductor process flow / action plan after process defect ID

22nm wide metal serpentine

Litho mask corrections (OPC)
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Overview of the test setup: dual prober + auto-loader, driven by NI tools
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The PXIe-4135 SMU at the heart of all param test
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Overview of the test setup: block diagram

- **PXI Chassis**: 4135 SMUs, etc
- **Switch**
- **Probe Card**
- **Wafer DUT**
- **Labview Controller**:
  - Test sequences
  - Data logging
  - GPIB-USB
- **Probe Station**
- **Wafer Loader**

Command path: MXI, GPIB interface

Signal path: TRIAX interface
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**Overview of the test setup: signal routing**

<table>
<thead>
<tr>
<th>SMU1 F-Hi</th>
<th>SMU2 F-Hi</th>
<th>SMU3 F-Hi</th>
<th>SMU4 F-Hi</th>
<th>DMM F-Hi</th>
<th>DMM F-LO</th>
<th>(Scope/LCR)</th>
<th>(Scope/LCR)</th>
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<td>4</td>
<td>5</td>
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<td>8</td>
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</table>

**SWITCH FORCE BANK**

<table>
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</table>

**SWITCH SENSE BANK**

**PROBE CARD**
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Process experiment / test scenario: Impact of 3D processing on FinFET devices

- A CMOS FinFET wafer has undergone 3D related process steps: bonding, extreme thinning, TSV introduction from wafer back-side & RDL
- same devices are tested before and after 3D processing to monitor its potential impact on FinFET
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Process experiment / test scenario: Impact of 3D processing on FinFET devices

B3D: results before 3D process steps
A3D: results after 3D process steps
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Other commonly used test scenario’s
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Benchmark results with 4135 SMUs

+ test results with PXIe-4135 SMUs
- test results with high-end third-party tools

Off-state / On-state transistor current measurements: excellent match!

Transistor gate sweeps (currents < pA): excellent match!

Low-capacitance CV measurements for transistor gates: excellent match!!
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Data logging/query/analysis

- SAS based data warehouse
- Web Interface for data query
- Contains all imec metrology data
- Die index standardization \(\rightarrow\) overlay
- Calculations on datasets

\[\text{HEADER}\]

- \text{Begin Of Data}
- \text{First Die Coordinate}
- \text{TimeStamp Datapoint}

- CSV

\[\text{Galaxy Examinator Pro}\]
Future work

NI tool related challenges

- Expand Labview parametric test procedure library
  - Transistor Ring Oscillators (Power Delay)
  - SRAM cells (Butterfly curves, SNM)
  - Transistor reliability / degradation tests
- ... 
- Faster measurements (Source delay, Aperture time, ...)

Probe tool related challenges

- Technology nodes scale ➔ probe pads/µbumps scale, higher pad/pin counts ➔ probe to wafer alignment
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