From the Designers: DC Measurement Considerations

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PXle-4081: 7 ½ Digit DMM
- 1,000 V input
- 12 ppm voltage accuracy
- Up to 1.8 MS/s acquisition

PXle-4135: Low Current SMU
- 200 V source and measure
- 10 fA current sensitivity
- Up to 1.8 MS/s acquisition

PXle-4309: 8-channel Nanovoltmeter
- 0.1 V to 15 V ranges
- < 100 nV sensitivity
- Up to 2 MS/s acquisition
NI Measurement Fundamentals Documentation

NI-DCPower and NI-DMM Driver Help Files

Whitepapers and practical guides
Parasitic Loading Effects
(Remote Sense, Offset Compensation & Guarding)
Remote Sense and Guarding

- Remote Sense: compensates for voltage drop due to parasitic resistances
  - Ideal for high current CV, low resistance measurement

- Voltage Offset Compensation: Adjusts for parasitic thermocouples
  - Ideal for low voltage / low resistance measurements

- Guarding: minimizes leakage current and capacitance effects of cable
  - Ideal for low current (< 1 nA) measurements
Local Sense (2-wire)

Voltage at connector is controlled to 5 V

Voltage drops due to lead resistance

DUT does not see full voltage

<table>
<thead>
<tr>
<th>DUT Impedance</th>
<th>DUT Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 kΩ</td>
<td>4.99 V</td>
</tr>
<tr>
<td>100 Ω</td>
<td>4.9 V</td>
</tr>
<tr>
<td>10 Ω</td>
<td>4.16 V</td>
</tr>
<tr>
<td>1 Ω</td>
<td>1.67 V</td>
</tr>
</tbody>
</table>
Local Sense (2-wire) with $R_{lead}$ Compensation

Virtual negative resistance

$$-(R_{Hi} + R_{LO})$$

Requires well characterized and stable lead resistances.

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</table>
Remote Sense (4-wire)

High impedance wires sense voltage directly at DUT

DUT voltage is directly controlled to 5 V

SMU
Low Resistance Measurements Technique

Current Reversal (Offset Compensated Ohms)

Uncompensated:

\[
R_{\text{meas\_ideal}} = \frac{I_{\text{test}} \times R_{\text{actual}}}{I_{\text{test}}} = R_{\text{actual}}
\]

\[
R_{\text{meas\_actual}} = \frac{I_{\text{test}} \times R_{\text{actual}} + V_{\text{emf}}}{I_{\text{test}}} = R_{\text{actual}} + \frac{V_{\text{emf}}}{I_{\text{test}}}
\]
Low Resistance Measurements Technique

Current Reversal (Offset Compensated Ohms)

Continuous Compensation:

Looping sequence of +/- I setpoints

\[ V_{m1} @ I = + I_{test} \]
\[ V_{m2} @ I = - I_{test} \]
\[ \ldots \]

\[ R_{meas} = \frac{(V_{m1} - V_{m2})}{2 \times I_{test}} \]

\[ R_{meas} = \frac{(I_{test} \times R + V_{emf} - (-I_{test} \times R + V_{emf})}{2 \times I_{test}} \]

\[ R_{meas} = \frac{(2 \times I_{test} \times R)}{2 \times I_{test}} = R \]

(DMMs achieve O.C.O. by switching current source between \( I_{test} \) and 0A)
Guarding to Minimize Leakage

- SMU
- HI
- LO
- GUARD
- 100V
- 10 Ω
- 1 Ω
- PCB
- DUT
Guarding to Minimize Capacitive Effects of Cabling

10 nA range (HI)

100V / $R_{DUT}$ = 1 nA
Guarding to Minimize Capacitive Effects of Cabling

GUARD sources current > 10 nA range, charges stray capacitance in cable and PCB ~10000x faster, HI sees virtually no capacitance due to $V_{HI} \approx V_{GUARD}$.
Guarding and Remote Sense Through a PCB
Coaxial Cables (Non-Guarded)

\[ V_{HI} \neq V_{LO} \Rightarrow I_L \] (leakage current)
Triaxial Cables (Guarded)

$$V_{HI} = V_{GUARD} \implies I_L \sim 0$$
Noise
(Specs, Sources, Shielding and Rejection)
# Noise on SMU Spec Sheets

## Voltage Programming and Measurement Accuracy/Resolution

### Table 2. Voltage Programming and Measurement Accuracy/Resolution

<table>
<thead>
<tr>
<th>Range (0.1 Hz to 10 Hz, peak to peak), Typical</th>
<th>Noise (0.1 Hz to 10 Hz, peak to peak), Typical</th>
<th>Accuracy (23 °C ± 5 °C) ± (% of voltage + offset)</th>
<th>Tempco ± (% of voltage + offset)°C, 0 °C to 55 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 mV</td>
<td>100 mV</td>
<td>2 μV</td>
<td>0.02% + 50 μV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.02% + 50 μV</td>
<td>0.016% + 30 μV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.02% + 50 μV</td>
<td>0.0005% + 1 μV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 μV</td>
<td>0.02% + 300 μV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.02% + 300 μV</td>
<td>0.016% + 90 μV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60 μV</td>
<td>0.02% + 3 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.02% + 3 mV</td>
<td>0.016% + 900 μV</td>
</tr>
</tbody>
</table>

### Figure 2. Voltage Measurement Noise vs. Measurement Aperture, Nominal

- **Noise**: Wideband source noise
- **<20 mV peak-to-peak in 60 V range, device configured for normal transient response, 10 Hz to 20 MHz, typical**
Noise

- Noise sources
  - Thermal noise
  - EMI noise (RF, LF / Power Line, Electrostatic)
  - ADC noise
  - 1/f noise
  - Common mode current noise
Thermal noise (White Noise)

\[ E_{th} = \sqrt{4kTR} \]

Noise Voltage spectrum is flat vs frequency.
Noise rms = en*sqrt(BW).
Noise p-p approx 5.5*Noise rms.
Uncorrelated noise sources add by RSS!!
Noise increases with R. Set your expectations accordingly!!
Theoretical Limits of Voltage Measurements

- For bandwidths up to 10Hz...

EMI Noise Sources
Minimizing Magnetic Field Loop Antennas

External sources generate magnetic fields that couple via loop area

Can be mitigated by minimizing or eliminating pickup loop area and employing twisted cabling
EMI Noise Sources
Shielding to Minimize Electrostatic Coupling

External signals couple charge into cables

1 MOhm

\[ V_{AC} \]

\[ I_{AC} \]

\[ C_{stray} \]

DMM / SMU

Frequently a human body
EMI Noise Sources
Shielding to Minimize Electrostatic Coupling

External signals shunted to ground through the shield

1 MΩ

\[ C_{\text{stray}} \]

\[ V_{\text{AC}} \]
EMI Noise Sources
Shielding to Minimize Electrostatic Coupling

external signals shunted to ground through the shield

1 MOhm

DMM / SMU

$V_{AC}$

$I_{AC}$

$C_{stray}$
Cables

unshielded banana cables

shielded banana cables w/ Teflon insulator

Low noise triax cables
Power Line Noise

Any noise related to the power grid frequency (50/60Hz)

- Can be the dominant noise source for low level measurements
- Rejection achieved by integrating over integer Power Line Cycles (PLCs)
  - Notch filter rejection

Common sources of power line noise
- Power supplies
- Light sources
- Other equipment in racks
Noise Rejection Techniques

The following figure shows the resulting noise rejection as a function of frequency.

**FIRST ORDER**

**SECOND ORDER**
1/f Noise

- Frequently dominated by instrument components
- Requires long timescales to observe

**Pink Noise (1/f amplitude)**

**Time Domain**

**FFT**

Power spectrum varies inversely

**White Noise (constant amplitude)**

**Time Domain**

**FFT**

Power spectrum does not vary
Common Mode Current Noise

NON-ISOLATED  |  ISOLATED

ADC

VOLTAGE  CURRENT

HI  LO
Common Mode Current Noise

NON-ISOLATED

ISOLATED

ADC

+ -

VOLTAGE CURRENT

HI

LO

Z?

Z?

Z?
Drift

(Temperature, Dielectric Absorption & Calibration)
Temperature

- Everything changes with temperature
  - R: 5-25ppm/C (thin film) to 250ppm/C (thick film) to 5000ppm/C (carbon)
    - Copper: 0.4%/C!
  - V: -2mV/C (PN diodes), ~2-3mV/C (low voltage zener diodes)
  - C: 30ppm/C (C0G) to several%/C
- Including your instrumentation
  - … and your DUT
Temperature Drift
Building A/C kicks in at 5AM
Temperature Drift Comparison (10nA Ranges)

Other products with 10nA ranges
Thermocouples

- A voltage gradient appears across a material when a temperature gradient is applied
  - Seebeck voltage – uV/C
  - Magnitude varies with material
- Common parasitic thermocouples
  - relays, connectors, IC pins…
  - Air movement results in temperature fluctuation, which looks like low frequency noise
- Think about where your heat is being generated
  - Limit temperature gradients to similar materials
  - Don’t add gradients of your own!
  - If gradient / junction can’t be avoided, have matching isothermal junctions in HI/LO paths.
- Block air flow
Dielectric Absorption

- After a C is charged, dielectric molecules torqued to align with field (slowly)
  - This costs energy
  - Releases energy when discharging/re-aligning
    - “Bonus” capacitance! Fraction of total C
- The most annoying parasitic that I’m aware of
  - Almost never specified
  - Very difficult to characterize / compensate for
  - Slows everything down

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Rule-of-thumb DA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>~0%</td>
</tr>
<tr>
<td>Ceramic: C0G/NP0</td>
<td>&lt; 0.1%</td>
</tr>
<tr>
<td>Ceramic: X7R</td>
<td>1-2%</td>
</tr>
<tr>
<td>Tantalum</td>
<td>5-10%</td>
</tr>
<tr>
<td>Electrolytic</td>
<td>&gt;10%</td>
</tr>
</tbody>
</table>
DA in action – 100nF ceramic
Dielectric Absorption

- Also occurs in capacitors you didn’t even want
  - Cables (PVC Insulation)
  - Connectors (PA / Nylon / Polyamide)
  - PCBs

- What can you do?
  - Choose capacitors with lower DA ($$)
  - Optimize the test sequence such that you would charge the capacitor while performing other tests
    - Don’t measure sleep current’s first
  - Guarding (minimize parasitic C’s)
Calibration & Drift

External Cal

Corrects for:
• Long term time drift in onboard references
• Any offsets self cal can’t access

Self Cal

Corrects for:
• Short term gain / offset drift not related to references.
  • Temperature drift
  • Less stable components
Self Calibration: Impact on Temperature Drift

**Temperature** (from module temp sensor)

$T_{ambient}$: 23 to 55 to 0 to 23 deg C

**voltage offset error**
Self Calibration: Impact on Temperature Drift

Temperature (from module temp sensor)

\[ T_{ambient} : 23 \text{ to } 55 \text{ to } 0 \text{ to } 23 \text{ deg C} \]
Self Calibration: Impact on Temperature Drift

Temperature (from module temp sensor)

$T_{\text{ambient}}$: 23 to 55 to 0 to 23 deg C

Voltage offset error

Self-calibration applied

This spec is not the tempco of the instrument, it is the tempco of the accuracy spec.
Questions